REMARKS

Claims 1-28 are pending in this application. By this response to the non-final Office Action dated December 7, 2009, independent claims 1, 8, 13, 20, 27, and 28 are amended. An example of the support for the limitations added by this amendment is illustrated by the Declaration of Korbin Van Dyke filed on May 29, 2007 in U.S. Patent App. Ser. No. 10/757,515 (now issued as U.S. Patent No. 7,430,655), in particular sections 21-27 thereof. The present application discloses the same materials cited by the Declaration of Korbin Van Dyke. A copy of this declaration is attached to this Amendment for the Examiner's convenience as Attachment A. Favorable reconsideration of the application in light of the foregoing amendments and following comments is respectfully solicited.

I. The Present Application has a Valid Claim of Priority Under 35 U.S.C. § 120 to the Filing of U.S. Patent App. Ser. No. 08/516,036

Through operation of 35 U.S.C. § 120, the present application has a valid claim of priority of the August 16, 1995 filing date for U.S. Patent App. Ser. No. 08/516,036.

Section 2 of the Office Action incorrectly concluded that

> The disclosure of the prior-filed application, Application No. 09/169,963, fails to provide adequate support or enablement in the manner provided by the first paragraph of 35 U.S.C. § 112 for one or more claims of this application. Claims 1-28 are not supported by this Application. For example, Application No. 09/169,963 does not adequately support catenating multiple arithmetic results from a single instruction. The Applications 09/169,963, 08/754,827 and 08/516,036 are not available under 35 U.S.C. 120. . . .
>
> *(emphasis added)*

It appears that the Office Action makes reference to the following language recited in each of independent claims 1, 8, 13, 20, 27, and 28:

> a single . . . instruction that specifies a[n] . . . arithmetic operation to cause multiple instances of the . . . arithmetic operation to be performed, each instance of the . . . arithmetic operation to be performed using a different one of the plurality of multiple-bit data elements in partitioned fields of at least one of the registers to produce a catenated result.

On pages 15-16 of the Declaration of Craig Hansen Under 37 CFR § 1.131 filed with Applicants' previous response, in section 1.4 of the table provided thereon, inventor Hansen explained that a "group add" instruction, such as the group add operation shown in Exhibit A1, MU0020388 accompanying his declaration, was an example of the recited "single . . . instruction." U.S. Patent App. Ser. No. 09/169,963 also discloses the recited "single . . . instruction," and provides full support for the claimed subject matter. Support is found, for example, in U.S. Patent App. Ser. No. 09/169,963 by a Group Add operation described on pages 49, 50, 54, and 103-109 of the Microfiche Appendix included in U.S. Patent App. Ser. No. 09/169,963, "the contents of which [were] hereby incorporated by reference" (U.S. Patent No. 6,006,318, col. 14, lines 6-9). A copy of these pages of the Microfiche Appendix, as included in U.S. Patent App. Ser. No. 08/516,036, is attached to this Amendment as Attachment B for the Examiner's convenience. This same disclosure of a Group Add operation, which discloses an example of the recited "single . . . instruction," was presented continuously through the chain of continuity provided by U.S. Patent App. Ser. Nos. 08/516,036, 08/754,827, and 09/169,963.

Thus, the Office Action was incorrect in its conclusion that these applications, to which the present application claims the benefit of priority, do not adequately support the claimed "single . . . instruction." Likewise, Applicants respectfully note that these applications, when their disclosures are properly considered in their entireties, support the claimed subject matter. Accordingly, the claimed subject matter has a valid claim of priority to the August 16, 1995 filing date for U.S. Patent App. Ser. No. 08/516,036.

II. Rejection Under 35 U.S.C. § 103(a) in View of Cray and Matsuura

In section 6 of the Office Action, claims 1, 6-8, 12, 13, 18-20, and 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cray, Jr. (U.S. Patent No. 4,128,880, herein referred to as Cray) in view of Matsuura et al. (U.S. Patent No. 4,725,973, herein referred to as Matsuura). Applicants respectfully traverse.

Independent claims 1, 13, 27, and 28 each recite, *inter alia*,

> an execution unit coupled to the data path, the execution unit configured to execute a plurality of instruction streams from the plurality of threads in a multistage pipeline such that the multistage pipeline is capable of including instructions from different ones of the instruction streams in different stages of the multistage pipeline.

Independent claims 8 and 20 each recite, *inter alia*,

> an execution unit coupled to the data path, the execution unit configured to execute first and second instruction streams from the first and second threads, respectively, in a multistage pipeline such that the multistage pipeline is capable of including instructions from different ones of the instruction streams in different stages of the multistage pipeline.

In embodiments of the above limitations, costly save/restore operations of the vector register state can be avoided when switching between threads. In contrast, the Cray and Matsuura systems do not disclose or render obvious the recited multistage pipeline, and accordingly require save/restore operations of the vector register state when switching between threads.

Further, independent claims 1, 8, 13, 20, 27, and 28 each recite, *inter alia*,

> the single . . . instruction causing a plurality of multiple-bit data elements in partitioned fields to be read in parallel from a register included in the register file, and causing the catenated result to be written in parallel to one of the registers included in the register file.

However, the instructions performed by the Cray and Matsuura systems do not cause reading from and writing to registers included in the register file in parallel as recited. For

example, although Matsuura, col. 3, lines 29-31 states that "a vector register must simultaneously read or write n elements during the time period of one cycle," in Matsuura, FIG. 4 it can be seen that the elements are transferred separately over the course of the four 1/4-cycle internals T0 to T1, T1 to T2, T2 to T3, and T3-T0.

For at least the above reasons, independent claims 1, 8, 13, 20, 27, and, 28, and claims 6, 7, 12, 18, 19, and 24-28 which depend thereon, are not obvious in view of the cited art. Accordingly, Applicants respectfully request withdrawal of the rejection under Section 103(a) set forth in section 6 of the Office Action.

III. Rejection Under 35 U.S.C. § 103(a) in View of Cray, Matsuura, and Laudon

In section 12 of the Office Action, claims 2-5, 9-11, 14-17, and 21-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cray in view of Matsuura and further in view of Laudon et al., "Interleaving: a Multithreading Technique Targeting Multiprocessor and Workstations" (herein referred to as Laudon). Applicants respectfully traverse.

As explained in Section I above, the claimed subject matter to the August 16, 1995 filing date for U.S. Patent App. Ser. No. 08/516,036. As discussed on page 21 of Applicant's last response, Laudon has a publication date of October 1994 – less than one year prior to the priority date for his application.

Thus, Laudon is not available as prior art under Section 102(b), and section 4 of the Office Action was incorrect in concluding that the statutory bar of Section 102(b) applies to Laudon. Thus, the declarations submitted under Rule 131, demonstrating conception of the claimed subject matter prior to October 1994 and the exercise of due diligence, is effective in establishing that Laudon is not valid prior art for the claimed subject matter. Applicants

respectfully request full consideration of the remarks presented in Section II of Applicants' last response (presented on pages 20-24 thereof) and declarations and exhibits submitted in support thereof.

For the Examiner's convenience, in view of the incorrect conclusion reached in section 2 of the Office Action that the prior disclosure does not adequately support catenating multiple arithmetic results from a "single . . . instruction" as recited in each of the independent claims, Applicants wish to note that on pages 15-16 of the Declaration of Craig Hansen Under 37 CFR § 1.131 filed with Applicants' previous response, in section 1.4 of the table provided thereon, inventor Hansen explained that a "group add" instruction, such as the group add operation shown in Exhibit A1, MU0020388 accompanying his declaration, was an example of the recited "single . . . instruction." For the Examiner's convenience, Attachment C to this response includes pages MU0020371, MU0020373, and MU0020388 of Exhibit A1 included with the Declaration of Craig Hansen Under 37 CFR § 1.313, and Attachment D to this response includes pages of Exhibit A2 included with the Declaration of Craig Hansen Under 37 CFR § 1.313. These each relate to the "group add" operation and provide evidence of the inventors' conception of the recited "single . . . instruction" prior to October 1994. In particular, MU0020388 discloses that catenated data a/b/c/d is added to catenated data e/f/g/h to produce a catenated result a+e/b+f/c+g/d+h

With respect to the limitations relating to the multistage pipeline added to the claims by this Amendment, Applicants again refer the Examiner to Attachment A to this response (Declaration of Korbin Van Dyke filed on May 29, 2007 in U.S. Patent App. Ser. No. 10/757,515). Section 24 thereof explains how the description of the Zeus Superspring pipeline provides supporting disclosure of a "multistage pipeline such that, at a given time, the multistage

pipeline includes instructions from different ones of the instruction streams in different stages of the multistage pipeline." Pages MU0023250-52 of Exhibit A2 included with the Declaration of Craig Hansen Under 37 CFR § 1.313, which are included in Attachment D to this response for the Examiner's convenience, in the section entitled "Pipeline Organization" discloses similar material, and provides evidence of the inventors' conception prior to October 1994 of the use of "a multistage pipeline such that, at a given time, the multistage pipeline is capable of including instructions from different ones of the instruction streams in different stages of the multistage pipeline," as recited in the claims.

With respect to the limitations relating to the single arithmetic instruction causing reading from and writing to registers included in the register file in parallel, an example of evidence of the inventor's conception prior to October 1994 is provided on pages MU0023311-12 of Exhibit A2 included with the Declaration of Craig Hansen Under 37 CFR § 1.313, which are included in Attachment D to this response for the Examiner's convenience. These pages indicate, for example:

```
case op of
. . .
        G.ADD . . .:
                a <- REG[ra]
                b <- REG[rb]
. . .
case op of
        G.ADD:
                for i <- 0 to 128-size by size
                        c_{i+size-1..i} <- a_{i+size-1..i} + b_{i+size-1..i}
                endfor
```

As explained in Section II above, Cray and Matsuura do not render obvious independent claims 1, 8, 13, and 20. Thus, claims 2-5, 9-11, 14-17, and 21-23, which depend thereon, are not rendered obvious by Cray and Matsuura. Laudon, as discussed above, is not available as prior

art against the claimed subject matter. Thus, Applicants respectfully request withdrawal of the rejection under Section 103(a) set forth in section 12 of the Office Action.

IV. Conclusion

In view of the foregoing, Applicants submit that all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at telephone number indicated below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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